UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/424,966	03/06/2000	AKIHIDE SHIBATA	247322001700	8894

25226 7590 03/17/2003

MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO, CA 94304-1018

EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/424,966	SHIBATA ET AL.	
	Examin r	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *4,5,7,9,11,13,15,17,19,21,23,25,27 and 29-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 3-6, the phrase "a gate terminal fabricated on a channel region which receives a first input signal, wherein the channel region is formed between said source region and drain region and receives the first input signal through a gate insulating film". It is well known in the semiconductor art that a conducting channel would be formed between the source and drain regions when a voltage is applied to a gate electrode. The conducting channel would have a voltage different from that of the gate electrode. Therefore, it is unclear how the channel region receives the first input signal from the gate electrode. It is believed that only the gate electrode receives the first input signal. The first input signal can only influence the channel region through the gate insulating film.

Claim 1 discloses each semiconductor element being provided with a single source region having a single source terminal and a single drain region having a single drain terminal in a well formed in a semiconductor layer, and a single gate terminal fabricated on a channel region. In addition, each of said semiconductor elements is electrically separated from the others. Then, it is unclear how a pair of a P-type semiconductor element and an N-type semiconductor element provided with one source region having one source terminal, one drain region having one drain terminal and a gate terminal in claims 6, 10, 18 and 22. There would be two source regions with two source terminals, two drain regions with two drain terminals and two gate terminals in a pair of a P-type

semiconductor element and an N-type semiconductor element in claims 6, 10, 18 and 22.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

3. Claims 1-3 insofar, as incompliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (Japanese patent application no. 08-204140).

In regards to claim 1, Okumura et al. show all the elements of the claimed invention in figs. 1-6. It comprises: a semiconductor device comprising a plurality of semiconductor elements (NMOS and PMOS of fig. 1), each being provided with a source region [105, 107] having a source terminal and a drain region [105, 107] having a drain terminal in a well [104, 106] formed in a semiconductor layer [104, 106], and a gate terminal [109] fabricated on a channel region and receives a first input signal, the channel region is formed between the source region and drain region, a gate insulating film [108] formed under the gate terminal [109], wherein: each of the semiconductor elements is electrically separated from the others; the well in each of the semiconductor elements is provided with a substrate terminal which receives a second input signal [111, 112] from a bias generator [207, 208] through a contact hole (see figs. 3 and 6) formed therein at a region other than the source region and drain region [105, 107].

Okumura et al. differ from the claimed invention by not showing the first and second input signals are different signals that are synchronized with each other. It would have been obvious for the first and second input signals are different signals that are synchronized with each other because they depend on the function of the circuit. Since the device structure of Okumura et al. is similar to that of the claimed structure, it is believed that the device of Okumura et al. is able to support a circuit that would require the first and second input signals having different signals that are synchronized with each other

In regards to claim 2, Okumura et al. inherently show the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, Okumura et al. show the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [102, 103].

4. Claims 1-3, 6, 8 and 14 insofar, as incompliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Iwamatsu.

In regards to claim 1, Chang et al. disclose a CMOS in fig. 1l. It comprises: a semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region [26, 34] and a drain region [23, 32] in a well [8, 12] formed in a semiconductor layer, and a gate terminal [20', 20"] fabricated on a channel region, the channel region is formed between the source region and drain region, a gate terminal formed on a gate insulating film [16, 18], wherein: each of the semiconductor

elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal region [28, 30] with a contact hole formed on it; regions [28, 30] are formed at regions other than the source region and drain region.

Chang et al. differ from the claimed invention by not showing a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements. In addition, Chang et al. further differ from the claimed invention by not showing each gate terminal receives a first input signal and each well receives a second input signal, and the first and second input signals are different signals that are synchronized with each other.

Iwamatsu shows a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements (PMOS and NMOS) in fig. 2. In addition, Iwamatsu further shows each gate terminal [5] receives a first input signal and each well [2, 3] receives a second input signal [V_{BG2}, V_{BG1}] in figs. 1-4. Fig. 4 shows the first input signal (V_{IN} is about 2.5 V) and the second input signals (V_{BG1} = V_{BG2} = CLK1 = CLK2 = 0 volt) are different signals that are synchronized with each other at a time interval.

Since both Chang et al. and Iwamatsu teach a CMOS structure with well contact regions for well voltages, it would have been obvious to have a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements of Iwamatsu in Chang et al. because they provide electrical connection between the semiconductor elements and the external circuit. It would also have been obvious to have the electrical connections of Iwamatsu in Chang et al. because they create a CMOS level shifter

circuit having a concise level shift and a low reduction in an integration degree. In addition, the electrical insulation layer [14] of Chang et al. insulates all the terminals of the PMOS, NMOS and the wells.

In regards to claim 2, the combined device inherently discloses the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, the combined device of Chang et al. and Iwamatsu shows the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [14 of Chang et al.].

In regards to claim 6, Chang et al. differ from the claimed invention by not showing a high potential is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal, and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal.

Iwamatsu shows showing a high potential V_{DD} is supplied to a source terminal of the PMOS and a low potential (ground) is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal V_{in}, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal when the clock voltages are 0 volt (CLK1=CLK2=0

volt), and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal V_{out} in figs. 1-4.

Since both Chang et al. and Iwamatsu teach a CMOS device, it would have been obvious to have the circuit connections and potentials of Iwamatsu in Chang et al. because they provide a CMOS level shifter circuit having a concise level shift and having a low reduction in an integration degree. In addition, the semiconductor structure of Chang et al. can support any desired CMOS wiring connections.

In regards to claim 8, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 8 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

In regards to claim 14, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 14 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

5. Applicant's arguments filed 1/3/03 have been fully considered but they are not persuasive.

It is urged, in pages 4-5 of the remarks, that claim 6 is clear and definite. However, as mentioned in the rejection, claim 1 discloses each semiconductor element being provided with a single source region having a single source terminal and a single drain region having a single drain terminal in a well formed in a semiconductor layer, and a single gate terminal fabricated on a channel region. It is unclear how a pair of a P-type semiconductor element and an N-type semiconductor element provided with one source region having one source terminal, one drain region having one drain terminal and a gate terminal in claims 6, 10, 18 and 22. There would be two source regions with two source terminals, two drain regions with two drain terminals and two gate terminals in a pair of a P-type semiconductor element and an N-type semiconductor element in claims 6, 10, 18 and 22.

It is urged, in pages 5-6 of the remarks, that the device of Okumura et al. can only receives fixed voltages and the p-type base region [104] cannot receive input signals of various levels, e.g., digital signals. Since the device structure of Okumura et al. is similar to the device of the claimed invention, it is believed that the device of Okumura et al. is able to support a circuit that would require the first and second input signals having different signals that are synchronized with each other.

It is urged, in page 6 of the remarks, that Chang et al. do not disclose or suggest a semiconductor device wherein the substrate receives a second input signal or the gate receives a first input signal, wherein the first and second signals are different signals that are synchronized with each other. However, as mentioned in the rejection, the combined device of Chang et al. and Iwamatsu shows each gate terminal receives a

first input signal and each well receives a second input signal [V_{BG2}, V_{BG1}]. In addition, fig. 4 of Iwamatsu shows the first input signal (V_{IN} is about 2.5 V) and second input signals (V_{BG1} = V_{BG2} = CLK1 = CLK2 = 0 volt) are different signals that are synchronized with each other at a time interval.

It is urged, in page 7 of the remarks, that V_{BG2} is a fixed positive voltage and V_{BG1} is a fixed negative voltage. However, as shown in fig. 4, V_{BG2} = CLK2 and V_{BG2} is varied from 0 volt to a positive voltage at a time interval. Fig. 4 also shows V_{BG1} = CLK1 and V_{BG2} is varied from 0 volt to a negative voltage at a time interval. Therefore, the combined device of Chang et al. and Iwamatsu teaches the limitation of the claimed invention.

6. Claims 22, 24 and 28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. Claims 10 and 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
March 15, 2003

Steven Loke
Primary Examiner
Steven Loke